REMARKS

The claims remaining in the present application are Claims 1-18. Claim 12 has been amended. Claims 14-18 have been added. No new matter has been added as a result of these amendments.

EXAMINER INTERVIEW SUMMARY

On July 7, 2004 Ronald Pomerenke, Anthony Murabito, and Bryn Ekroot, representatives for the Applicants conducted a telephonic interview with Examiners Chun Cao and Thomas Lee. Applicants thank the Examiners for granting this interview. United States Patent No. 5,812,860 to Horden et al. and U.S. Patent No. 6,118,306 to Orton were discussed with respect to Claim 1. The rejection under 35 U.S.C. §112, ¶1 enablement with respect to Claims 1-3 was discussed. The Examiners agreed that the rejection under 35 U.S.C. §112, ¶1 enablement with respect to Claims 1-3 would be removed. Applicants thank the Examiners for removing this rejection.

ALLOWABLE SUBJECT MATTER

Claim 12 is objected to but indicated as allowable if re-written to incorporate limitations from its base claim. Applicants have re-written Claim 12 in independent form, including all limitations from Claim 11, its base claim. Therefore, Applicants request allowance of Claim 12.

CLAIM REJECTIONS

35 U.S.C. §112

Claims 1-3 were rejected in the Office Action under 35 U.S.C. §112, ¶1, as failing to comply with the enablement requirement. This rejection has been removed per agreement in the above-referenced Examiner interview.

35 U.S.C. §103

Claims 1-3 are rejected under 35 U.S.C. §102(e) as being unpatentable over Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton) in view of Horden et al., U.S. Patent No. 5,812,860 (hereinafter, Horden). The rejection is respectfully traversed for the following reasons.

Currently Amended Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Independent Claim 1 recites that the core voltage is reduced to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor.

Applicants respectfully assert that Orton fails to teach or suggest reducing the voltage of the processor core to a value that is sufficient to

maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as claimed. Orton may purport to disclose a system that places a processor into a low activity state during which state may be preserved (col. 2, lines 44-60). However, Applicants respectfully assert that Orton does not teach or suggest that the voltage during this low activity state is insufficient to maintain processing activity. Therefore, Applicants assert that Orton fails to teach or suggest the limitations, "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor."

The cited combination of also fails because Horden fails to remedy the deficiencies in Orton in that Horden fails to teach or suggest the above claimed limitations. Applicants respectfully assert that the term "idle" in Horden's disclosure as understood by one or ordinary skill in the art does not mean that the processing activity is stopped. By idle, Applicants understand Horden to be referring to executing instructions in the processor at a frequency less than peak frequency. However, Horden is nevertheless executing instructions in the processor when applying Horden's so-called idle frequency/voltage pair and thus is maintaining processing activity. For example, Horden teaches that the operating system accumulates all processor need for all applications and directs a state machine to transition to a state that matches the frequency and voltage to the current application

needs. For example, if the current application mix does not require the peak performance level, the lowest state that will meet the application mix is used. (See., e.g., col. 4, lines 50-54; col. 3, lines 40-47).

Moreover, Horden provides an example of peak performance frequency of 32 MHz and an idle core frequency of 16MHz. Horden teaches that the minimum voltage *required to operate the processor at these frequencies* is provided to the processor (Horden, col. 3, lines 35-42). Applicants understand Horden to be teaching that processor activity is maintained at the idle frequency/voltage pair as the processor is being operated at 16MHz. In contrast, Applicants note that they have claimed that the system clock to the processor is disabled.

Applicants further note that Horden teaches that the operating system identifies whether the *core utilization and throughput* can be handled at the idle frequency or whether a higher frequency is required (Horden, col. 3, lines 48-53). This passage further indicates that Horden's idle frequency and voltage are used to maintain processor activity as Horden indicates that the idle frequency is capable of handling *core utilization and throughput.*

For the foregoing reasons, Claim 1 is neither taught nor suggested by the combination of Orton and Horden. Therefore, Applicants respectfully request allowance of Claim 1.

Claims 2-3 depend from Claim 1, which is believed to be allowable for the foregoing reasons. As a result of their dependency, Claims 2-3 are believed to be allowable. Applicants earnestly request their allowance.

35 U.S.C. §102

Claims 4-11 and 13 are rejected under 35 U.S.C. §102(a) or (e) as being anticipated by Orton. The rejection is respectfully traversed for the following reasons.

CLAIM 4

Currently Amended Claim 4 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by
>
> furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and
>
> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that Orton fails to teach or suggest these claim limitations.

Applicants have claimed that a feedback signal is applied to the voltage regulator. In Figure 1 of Orton, the voltage regulator (52) is depicted with an input signal from the host bridge (18). However, Applicants do not understand the voltage regulator to receive a feedback signal, as Applicants have claimed.

In Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to be feedback signals, as claimed.

Furthermore, Applicants do not understand either of these signals (VR_LO/HI#, VR_ON) to reduce the output voltage of the voltage regulator below a specified output voltage, as claimed.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by Orton. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable.

Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 is neither taught nor suggested by Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 8-10 depend from Claim 7. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 8-10 to be allowable.

Claim 11

Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...

means for reducing the selectable voltage below a level provided by the voltage regulator (emphasis added).

The limitations "the selectable voltage below a level provided by the voltage regulator" describe a selectable voltage level that is below the lowest voltage level which the voltage regulator is specified to output.

Orton may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Orton is silent as to causing the voltage regulator to output a voltage below the lowest voltage level that the voltage regulator is specified to output. Applicants respectfully assert that one of ordinary skill in the art would understand Orton to teach that the output voltage of the voltage regulator to be within a range specified by the voltage regulator, as Orton is silent as to causing the voltage regulator to output a voltage outside of that range.

For the foregoing reasons, Applicants respectfully assert that Orton fails to teach or suggest the limitations, "reducing the selectable voltage below a level provided by the voltage regulator." Therefore, Applicants earnestly request allowance of Claim 11.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Claim 13 recites circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases. Claim 13 further recites means for enabling this circuitry. Thus, limitations of Claim 13 recite that the circuitry for conserving charge stores charge from the voltage regulator.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. The rejection asserts that Orton teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Orton does not teach or suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Orton fails to teach or suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

NEW CLAIMS

Claims 14-18 have been added. Support for Claims 14-18 may be found in the instant specification at least at page 7, line 3 - page 11, line 11. No new matter has been added as a result of these claim amendments.

Claim 14 recites:

> A circuit for providing a regulated voltage to a processor comprising:
>
> a voltage regulator having:
> an output terminal providing a selectable voltage, and
> an input terminal for receiving signals indicating the selectable voltage level; and
> a voltage regulator feedback circuit;
>
> circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;
>
> a voltage source furnishing a value higher than the selectable voltage; and
>
> a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

Applicants respectfully assert that the prior art fails to teach or suggest the limitations, "a voltage source furnishing a value higher than the

selectable voltage; and a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit."

Claims 15-17 depend from Claim 14, which is believed to be allowable for the foregoing reasons. Therefore, Claims 15-17 are believed to be allowable by virtue of this dependency.

Claim 18 depends from Claim 4, which is believed to be allowable for the foregoing reasons. Therefore, Claim 18 is believed to be allowable by virtue of this dependency.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-18 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
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